SOLID STATE SCIENTIFIC

SCM2114AL
1024 x 4 Static CMOS RAM

Preliminary

Features

- Fast Access Time Selection:
  100ns/120ns/150ns/200ns
- Direct Replacement for NMOS 2114 RAMs
- 883 Qualified Version: 883/2114ALM
- Three-State Outputs
- True TTL Compatibility
- Single 5V ± 10% Supply
- Fully Static Asynchronous Operation
- Three-State Outputs
- Common Data I/O Bus

Pin Configuration

A_6	1	18	V_{CC}
A_5	2	17	A_7
A_4	3	16	A_8
A_3	4	15	A_9
A_0	5	14	I/O_1
A_1	6	13	I/O_2
A_2	7	12	I/O_3
$\overline{CS}$	8	11	I/O_4
GND	9	10	$\overline{WE}$

Description

The SCM2114AL is a static silicon-gate CMOS RAM, a direct replacement for the NMOS 2114 4K RAM. The device is fully static and requires no clocks.

The Common Data lines (I/O) allow for simple interfacing with most microprocessors. A Chip Select input ($\overline{CS}$) is provided for memory expansion. The I/O lines are in a high impedance state when the chip is not selected ($\overline{CS}$ = 1). The Write Enable ($\overline{WE}$) is used to select either the read ($\overline{WE}$ = 1) or write ($\overline{WE}$ = 0) mode.

The SCM2114AL is fully socket and spec compatible with NMOS 2114 RAMS. For applications where $\overline{CS}$ and address access timing can be coincident, even lower power can be achieved using the SCM21C14 which features a standby current of 50µA max.

The SCM2114AL is available in industry standard 18 pin packages. The different versions of the SCM2114AL are outlined below.
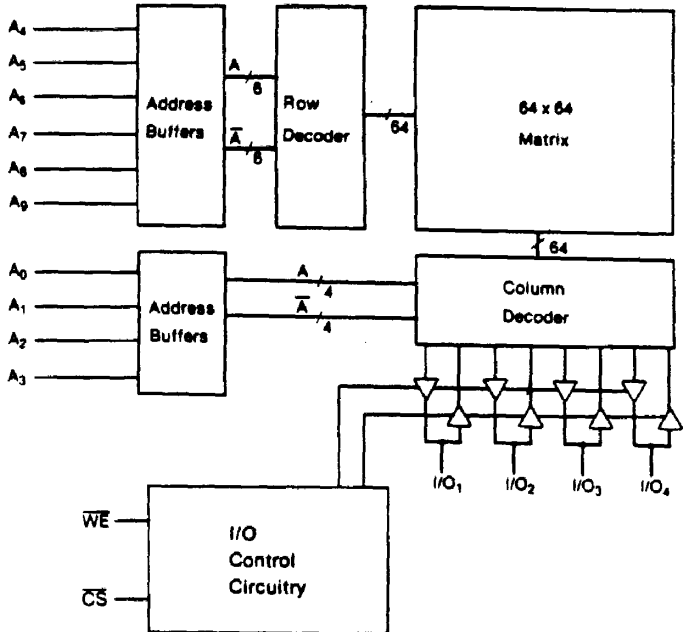
Block Diagram

Operating Characteristics Summary

Type	Access Time t_A (max.)	Operating Current I_{CC} (max.)
SCM2114AL-1	100ns	40mA
SCM2114AL-2	120ns	40mA
SCM2114AL-3	150ns	40mA
SCM2114AL-4	200ns	40mA
SCM2114ALM	200ns	50mA
883/2114ALM	200ns	50mA

SGS 2114AL
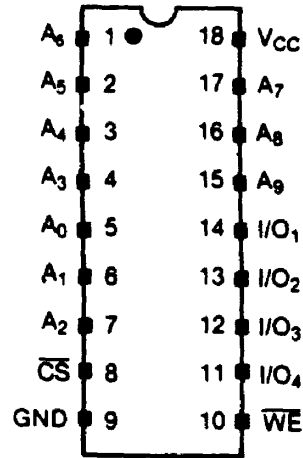
Absolute Maximum Limits

DC Supply Voltage (V_{CC}): -0.5 to $+6.0V$
Storage Temperature (T_S): $-65°$ to $+150°C$
Input Voltage (V_{IN}): ($V_{SS} - 0.3V$) $\leq V_{IN} \leq$ ($V_{CC} + 0.3V$)

Recommended Operating Conditions

Parameter	Limits
DC Supply Voltage (V_{CC})	5V ± 10%
Operating Temperature (T_A)	
2114AL-1/-2/-3/-4	0° to +70°C
2114ALM	−55° to +125°C

Pin Description

A_{0-9}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O_{1-4}	Data In/Out

Truth Table

$\overline{CS}$	$\overline{WE}$	I/O_{1-4}	Mode
1	X	High Z	Not Selected
0	1	Outputs	Read
0	0	Inputs	Write

D. C. Characteristics (V_{CC} = 5V ± 10%)

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions
I_{LI}	Input Current			1.0	μA	
I_{LO}	Output Leakage Current			1.0	μA	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = − 1.0mA
I_{CC}	Operating Current 2114AL		25	40	mA	V_{IH}/V_{IL} = 2.0/0.8V
I_{CC}	Operating Current 2114ALM		25	50	mA	V_{IH}/V_{IL} = 2.0/0.8V

A. C. Characteristics[2] (V_{CC} = 5V ± 10%)

Symbol	Parameter	2114AL-1 Min.	2114AL-1 Max.	2114AL-2 Min.	2114AL-2 Max.	2114AL-3 Min.	2114AL-3 Max.	2114AL-4/M Min.	2114AL-4/M Max.	Units
Read Cycle										
t_{RC}	Read Cycle	100		120		150		200		ns
t_A	Access from Address		100		120		150		200	ns
t_{CO}	Chip Select to Output Valid		50		70		70		70	ns
t_{CX}	Chip Select to Output Active	5		5		5		5		ns
t_{OTD}	Chip Select to Output Float		30		35		40		50	ns
t_{OHA}	Output Hold from Address Change	5		5		5		5		ns
Write Cycle										
t_{WC}	Write Cycle	100		120		150		200		ns
t_W	Write Pulse Width	50		70		90		120		ns
t_{DW}	Data Setup	50		70		90		120		ns
t_{DH}	Data Hold	0		0		0		0		ns
t_{OTW}	Write to Output Float		30		35		40		50	ns
t_{WR}	Write Recovery	0		0		0		0		ns

Read Cycle [3]
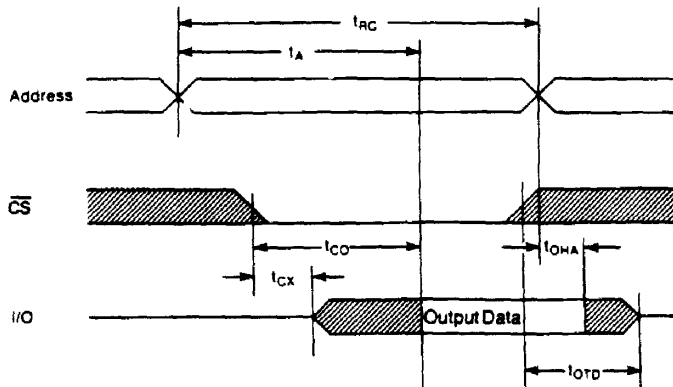
Write Cycle
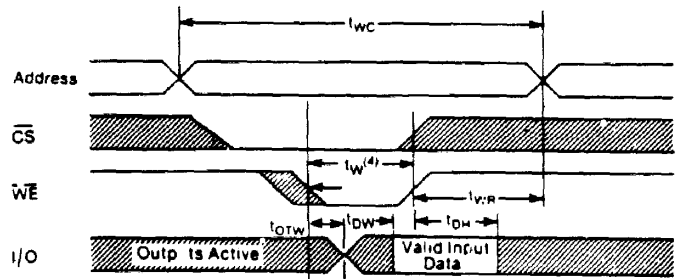
1. $T_A = 25°C$; $V_{CC} = 5.0V$
2. A.C. TEST CONDITIONS
   Input Pulse Levels: 0.8 to 2.4V
   Input Rise/Fall Times: ≤10ns
   Time Measurement
   Reference Level: 1.5V
   Output Load: 1 TTL Load and C_L = 100 pF

3. $\overline{WE}$ is high for a read cycle.
4. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high. $\overline{WE}$ must be high during address transitions.