CYPRESS SEMICONDUCTOR

1,024 x 4 Static R/W RAM

Features

- **Automated power-down when deselected (2148)**
- **CMOS for optimum speed/power**
- **Low power**
  - **—660 mW (commercial)**
  - **—770 mW (military)**
- **5-volt power supply ± 10% tolerance both commercial and military**
- **TTL-compatible inputs and outputs**

Functional Description

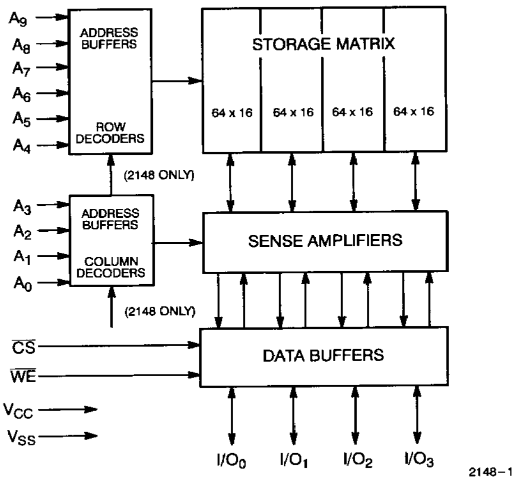
The CY2148 and CY2149 are high-performance CMOS static RAMs organized as 1024 by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The CY2148 and CY2149 are identical except that the CY2148 includes an automatic ($\overline{CS}$) power-down feature. The CY2148 remains in a low-power mode as long as the device remains deselected, i.e., ($\overline{CS}$) is HIGH, thus reducing the average power requirementsof the device. The chip select ($\overline{CS}$) of the CY2149 does not affect the power dissipation of the device.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location addressed by the address present on the address pins (A_0 through A_9).

Reading the device is accomplished by selecting the device, ($\overline{CS}$) active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins (A_0 through A_9) is present on the four data input/output pins (I/O_0 through I/O_3).

The input/output pins (I/O_0 through I/O_3) remain in a high-impedance state unless the chip is selected and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



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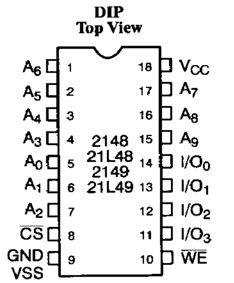
Pin Configuration



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Selection Guide (For higher performance and lower power refer to the CY7C148/9 data sheet)

		2148–35 2149–35	21L48–35 21L49–35	2148–45 2149–45	21L48–45 21L49–45	2148–55 2149–55	21L48–55 21L49–55
Maximum Access Time (ns)		35	35	45	45	55	55
Maximum Operating Current (mA)	Commercial	140	120	140	120	140	120
	Military			140		140	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		2148 2149 Min.	2148 2149 Max.	21L48 21L49 Min.	21L48 21L49 Max.	Units
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = −0.4 mA		2.4		2.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 8.0 mA			0.4		0.4	mA
V_{IH}	Input HIGH Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{OH}$, Output Disabled	T_A = 0°C to +125°C	−50	+50	−50	+50	μA
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \leq V_{IL}$ Output Open	T_A = 0°C to +70°C		140		120	mA
			T_A = −55°C to +125°C		140			
I_{SB}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS} \leq V_{IL}$ (2148 only)	T_A = 0°C to +70°C		30		20	mA
			T_A = −55°C to +125°C		30			
I_{PO}	Peak Power-On Current[3]	Max. V_{CC}, $\overline{CS} \leq V_{IL}$ (2148 only)	T_A = 0°C to +70°C		50		30	mA
			T_A = −55°C to +125°C		50			
I_{OS}	Output Short Circuit Current[4]	GND $\leq V_O \leq V_{CC}$	T_A = 0°C to +70°C		±275		±275	mA
			T_A = −55°C to +125°C		±350			

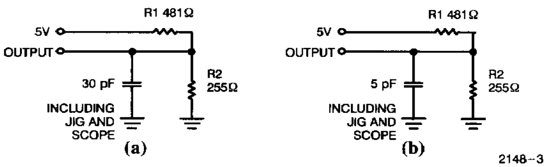
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise, current will exceed values give (CY2148 only).
4. For test purposes, not more than 1 output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



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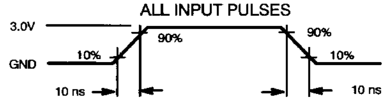

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Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[2]

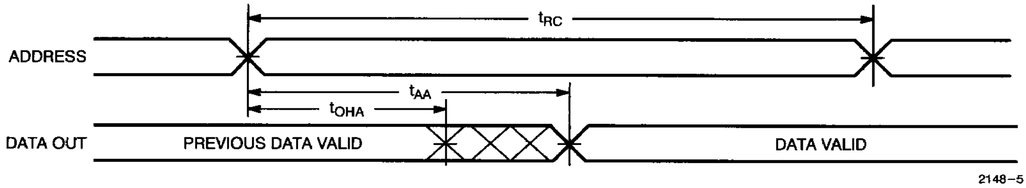
Parameters	Description		2148−35 2149−35 Min.	2148−35 2149−35 Max.	2148−45 2149−45 Min.	2148−45 2149−45 Max.	2148−55 2149−55 Min.	2148−55 2149−55 Max.	Units
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		35		45		55		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			35		45		55	ns
t_{ACS1}[6]	Chip Select LOW to Data Out Valid (CY2148 only)			35		45		55	ns
t_{ACS2}[7]				45		55		65	ns
t_{ACS}	Chip Select LOW to Data Out Valid (CY2149 only)			15		20		25	ns
t_{LZ}[8]	Chip Select LOW to Data Out Valid	2148	10		10		10		ns
		2149	5		5		5		
t_{HZ}[8]	Chp Select HIGH to Data Out Off		0	20	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		5		5		ns
t_{PD}	Chip Select HIGH to Power-Down Delay	2148		30		30		30	ns
t_{PU}	Chip Select LOW to Power-Up Delay	2149	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		35		45		55		ns
t_{WP}[9]	Write Enable LOW to Write Enable HIGH		30		35		40		ns
t_{WR}	Address Hold from Write End		5		5		5		ns
t_{WZ}[8]	Write Enable LOW to Output in High Z		0	10	0	15	0	20	ns
t_{DW}	Data-In Valid to Write Enable HIGH		20		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable LOW		0		0		0		ns
t_{CW}[9]	Chip Select LOW to Write Enable HIGH		30		40		50		ns
t_{OW}[8]	Write Enable HIGH to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		30		35		50		ns

Notes:

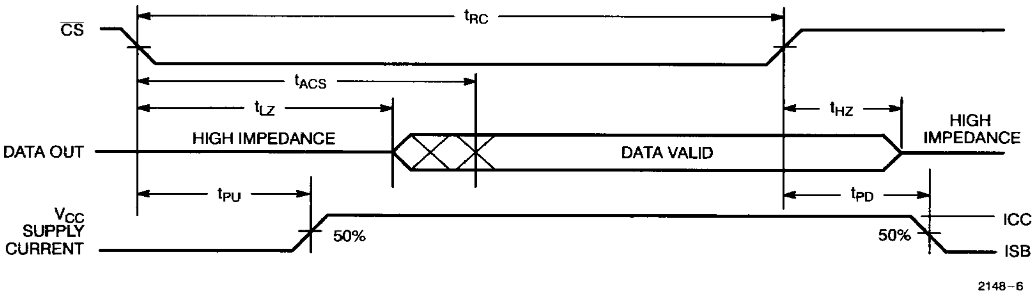
6. Chip deselected greater than 55 ns prior to selection.
7. Chip deselected less than 55 ns prior to selection.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in part (b) of AC Test Loads.
9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

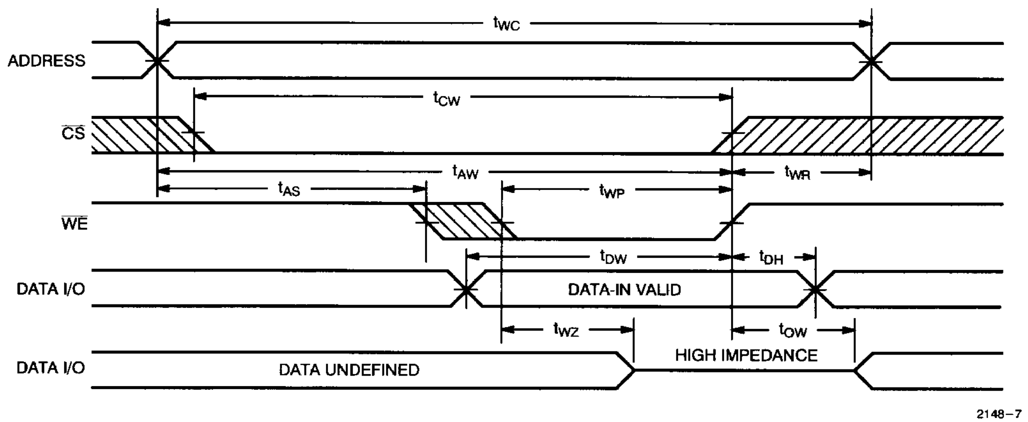
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled)

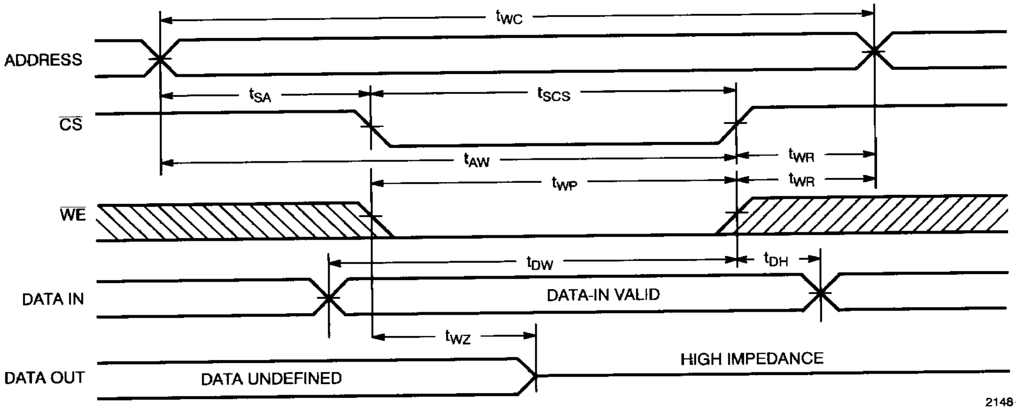


Notes:

10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS} = V_{IL}$.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 (CS Controlled) [13]



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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY2148−35PC	P3	Commercial
	CY2148−35DC	D4	
45	CY2148−45PC	P3	Commercial
	CY2148−45DC	D4	
	CY2148−45DMB	D4	Military
55	CY2148−55PC	P3	Commercial
	CY2148−55DC	D4	
	CY2148−55DMB	D4	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY2149−35PC	P3	Commercial
	CY2149−35DC	D4	
45	CY2149−45PC	P3	Commercial
	CY2149−45DC	D4	
	CY2149−45DMB	D4	Military
55	CY2149−55PC	P3	Commercial
	CY2148−55DC	D4	
	CY2148−55DMB	D4	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY21L48−35PC	P3	Commercial
	CY21L48−35DC	D4	
45	CY21L48−45PC	P3	Commercial
	CY21L48−45DC	D4	
55	CY21L48−55PC	P3	Commercial
	CY21L48−20DC	D4	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY21L49−35PC	P3	Commercial
	CY21L49−35DC	D4	
45	CY21L49−45PC	P3	Commercial
	CY21L49−45DC	D4	
55	CY21L49−55PC	P3	Commercial
	CY21L49−55DC	D4	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[14]	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[14]	7, 8, 9, 10, 11
t_{ACS2}[14]	7, 8, 9, 10, 11
t_{ACS}[15]	7, 8, 9, 10, 11
t_{OH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{WP}	7, 8, 9, 10, 11
t_{WR}	7, 8, 9, 10, 11
t_{DW}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11

Notes:
14. CY2148 only.
15. CY2149 only.

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